Docket No.: GR 98 P 1801

7/IDS E. Willis 12-14-99



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

Kai Wurster et al.

CIP of

Applic. No.

09/232,081, filed January 15, 1999

CIP filed

July 28, 1999

Title

Trench Capacitor with an Insulating Collar and Method for

Producing a Trench Capacitor

Group Art Unit

2811

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks, Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are cited herewith:

- U.S. Patent No. 5,187,550 (Yanagisawa), dated February 16, 1993;
- U.S. Patent No. 5,670,805 (Hammerl et al.), dated September 23, 1997;
- U.S. Patent No. 4,937,205 (Nakayama et al.), dated June 26, 1990;
- U.S. Patent No. 5,344,381 (Cabrera y Lopez Caram), dated September 6, 1994;
- U.S. Patent No. 5,336,912 (Ohtsuki), dated August 9, 1994;
- U.S. Patent No. 5,360,758 (Bronner et al.), dated November 1, 1994;
- U.S. Patent No. 5,250,829 (Bronner et al.), dated October 5, 1993;

Published European Patent Application No. 0 621 632 A1 (Rajeevakumar et al.), dated October 26, 1994;

"Shallow n^{*} Junctions in Silicon by Arsenic Gas-Phase Doping" (Ransom et al.), Journal of the Electrochemical Society, Vol. 141, No. 5, pages 1378-1381;

"Low Pressure Deposition of Doped SiO₂ by Pyrolysis of Tetraethylorthosilicate (TEOS) (Becker), Journal of the Electrochemical Society, Vol. 136, No. 10, pages 3033-3043;

"0.228μm² Trench Cell Technologies with Bottle-Shaped Capacitor for 1Gbit DRAMs" (Ozaki et al.), IEDM 95, pages 661-664.

Above-mentioned references cited in an Information Disclosure Statement submitted on April 22, 1999, in parent application No. 09/232,081.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

LAURENCE A. GREENBERG REG. NO. 29,308

Date: July 28, 1999

Lerner and Greenberg, P.A. Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100 Fax: (954) 925-1101

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